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Jinny Nguyen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	Date: August 30, 2006
Robert T. BAILIS et al.	Confirmation No: 5286
Serial No: 10/016,449	Group Art Unit: 2138
Filed: December 10, 2001	Examiner: John J. Tabone, Jr.

For: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER CLIENT WITHIN THE ASIC

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BRIEF ON APPEAL

Applicant submits this Appeal Brief pursuant to the Notice of Appeal filed in this case on July 26, 2006.

(1) Real Party in Interest

The real party in interest is International Business Machines Corporation by virtue of an assignment from the inventors recorded in the U.S. Patent Office on December 10, 2001, reel no. 012393, frame no. 0752.

(2) Related Appeals and Interferences

There are no related appeals, interferences, or judicial proceedings known to the Applicant.

(3) Status of Claims

Claims 1-9, 12, and 14-15 are pending in the application.

Claims 1-9 and 12, and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent. 6,829,751 to Shen et al. ("Shen").

All of the foregoing claims are being appealed.

(4) Status of Amendments

There are no unentered amendments.

(5) Summary of Claimed Subject Matter

Independent claim 1 recites an application specific integrated circuit (ASIC). The ASIC includes a standard cell including a plurality of logic functions. Specification, page 4, lines 13-22; FIG. 1. The ASIC further includes at least one bus coupled to at least a portion of the logic functions. Specification, page 4, lines 18-19; FIG. 1. The ASIC further includes a plurality of internal signals from the plurality of logic functions. Specification, page 4, line 23 – page 5, line 1; FIG. 1. The ASIC further includes a field programmable gate array (FPGA) coupled to the at least one bus and the plurality of internal signals. Specification, page 4, line 19 – page 5, line 1; FIG. 1. The field programmable gate array (FPGA) includes a debug client function that observes and manipulates the at least one bus and the plurality of internal signals. Specification, page 5, lines 5-8; FIG. 1. The debug client function is in communication with a server (see FIG. 2) and includes

comparator logic operable to compare selected ones of the plurality of internal signals coupled to the field programmable gate array (FPGA) with a trigger pattern downloaded from the server. Specification, page 6, lines 11-14; FIG. 2. The debug client function further includes storage logic operable to store a state of the selected ones of the plurality of internal signals that matches the trigger pattern for later retrieval by the server. Specification, page 6, lines 5-8; FIG. 2.

Independent claim 9 recites a debug client function within an application specific integrated circuit (ASIC). The debug client function is within a field programmable gate array (FPGA) (see FIG. 2), and includes external communicator logic in communication with a server. Specification, page 7, lines 1-2; FIG. 2. The debug client function further includes selector logic coupled to a plurality of internal signals that are internal to the application specific integrated circuit (ASIC) and are not exposed via an I/O pin. The selector logic provides each one of the plurality of internal signals coupled to the field programmable gate array (FPGA) at a particular input point within the debug client function. Specification, page 5, line 19 – page 6, line 2; page 2, lines 17-18; FIG. 2. The debug client function further includes comparator logic operable to compare selected ones of the plurality of internal signals at the particular input point with a trigger pattern downloaded from the server through the external communicator logic. Specification, page 6, lines 11-14; FIG. 2. The debug client function further includes storage logic operable to store a state of the selected ones of the plurality of internal signals that matches the trigger pattern for later retrieval by the server through the external communicator logic. Specification, page 6, lines 5-8; FIG. 2.

(6) Grounds of Rejection to be Reviewed on Appeal

Appellant requests review as to claims 1-9 and 12, and 14-15 and their rejection under 35 U.S.C. § 103(a) as being unpatentable over Shen.

(7) Argument

1. Claims 1-9, 12, and 14-15 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen.

(A) Claims 1-9, 12, and 14-15

Claim 1 recites an application specific integrated circuit (ASIC) including a field programmable gate array (FPGA) coupled to a plurality of internal signals (including at least one bus) within the ASIC. The FPGA includes a debug client function that is in communication with a server and includes comparator logic operable to compare selected ones of the plurality of internal signals coupled to the FPGA with a trigger pattern downloaded from the server, and includes storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

Shen fails to disclose several aspects of the claimed subject matter.

Shen discloses a system for designing an integrated circuit (IC) (see Abstract). More specifically, Shen discloses implementing an FPGA core that may be used to perform on-chip diagnostics that enable debugging functions, such as bus monitoring, probing, single step running, triggering, and capturing (col. 2, ll. 39-45).

(A)(i) Shen fails to disclose an FPGA having a debug client function that includes comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA with a trigger pattern downloaded from a server

The Examiner acknowledges that Shen fails to explicitly disclose an FPGA containing a debug client function including comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server. The Examiner, however, asserts that because Shen teaches monitoring the correctness of a bus protocol, detecting errors, and verifying bug fixes, then it would have been obvious to one of skill in the art that Shen possesses the claimed comparator logic. Further, the Examiner asserts that the functions of monitoring, verifying bug fixes, and detecting errors cannot be accomplished without "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server". Applicant respectfully disagrees.

While Shen discloses performing the functions of monitoring, verifying bug fixes, and detecting errors, Applicant submits that these functions are performed by the debugging workstation (or circuit) 104 (working with the FPGA core 106), which debugging workstation 104 is not contained within the FPGA core 102 (see col. 2, ll. 63-65; FIG. 1). That is, Shen discloses that data is collected from the FPGA core 106 and sent to the debugging workstation where the internal signals are analyzed (col. 3, ll. 52-57; col. 4, ll. 55-58).

Accordingly, because Shen discloses performing error detection (and analyzing internal signals) in the debugging workstation 104, Shen, therefore, teaches away from including comparator logic (as recited in claim 1) within an FPGA. Prior art references must be considered in their entirety, i.e., as a whole, including portions that would lead

away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

(A)(ii) Shen fails to disclose an FPGA having storage logic operable to store a state of selected ones of a plurality of internal signals that matches the trigger pattern for later retrieval by a server

In operation, Shen's FPGA core 116 (FIG. 3) is used to collect data from registers using a scan chain (col. 3, ll. 36-41). In particular, a user decides which signals need to be observed during a debugging period and, accordingly, the FPGA generates select signals (e.g., DIAG_SEL10 and DIAG_SEL11) that control which scan segments (of the scan chain) need to be accessed (col. 5, ll. 30-33; col. 4, ll. 35-58). After data is collected from the scan chains, the data is compressed and sent to a debugging workstation (col. 3, ll. 52-54). Thus, Shen discloses storing only signals within the FPGA core 116 that are pre-selected by a user, and not signals that match a trigger pattern.

In addition, while Shen discloses that the system 100 is operable to search for a specific signal pattern (see col. 6, l. 11), Shen is silent as to specifically *how* the signal pattern is searched. Based on the above, Applicant respectfully submits that Shen's debugging workstation 104 performs the function of searching for a specific signal pattern based on data collected from the FPGA core 116. Thus, Shen fails to disclose an FPGA including storage logic operable to store a state of the selected ones of the plurality of internal signals that matches the trigger pattern for later retrieval by the server.

Accordingly, Applicant respectfully submits that claim 1 is, therefore, improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over Shen.

Independent claim 9 incorporates the features of claim 1 and is, therefore, also improperly rejected for at least the same reasons. Claims 2-8, and 12, 14-15 respectively

depend from claims 1, and 9, and are also improperly rejected for at least the same reasons.

Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 50-0563 (IBM Corporation).

Respectfully submitted,
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August 30, 2006
Date

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Appendix of Claims

1. (Previously Presented) An application specific integrated circuit (ASIC) comprising:

a standard cell including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable gate array (FPGA) coupled to the at least one bus and the plurality of internal signals, the field programmable gate array (FPGA) including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals, the debug client function being in communication with a server and including,

comparator logic operable to compare selected ones of the plurality of internal signals coupled to the field programmable gate array (FPGA) with a trigger pattern downloaded from the server; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

2. (Previously Presented) The ASIC of claim 1, wherein the at least one bus comprises an internal bus, the internal bus being internal to the ASIC and not being exposed via an I/O pin.

3. (Previously Presented) The ASIC of claim 2, wherein the server comprises a debugger server running a debugger application.

4. (Previously Presented) The ASIC of claim 3, wherein the debug client function is programmed by the debugger server.

5. (Previously Presented) The ASIC of claim 1, wherein the debug client function further includes:

external communicator logic for receiving and transmitting information to the server;

selector logic coupled to the at least one bus and the plurality of internal signals, the selector logic to provide each one of the plurality of internal signals coupled to the field programmable gate array (FPGA) at a particular input point within the debug client function; and

interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween.

6. (Previously Presented) The ASIC of claim 5, wherein the interface logic comprises:

the storage logic;

the comparator logic, wherein the comparator logic is coupled to the storage logic; and

output logic coupled to the comparator logic for controlling the plurality of internal signals on the ASIC.

7. (Previously Presented) The ASIC of claim 4, wherein the server utilizes the debug client function to debug hardware within at least one of the plurality of logic functions.

8. (Previously Presented) The ASIC of claim 4, wherein the server utilizes the debug client function to debug software within at least one of the plurality of logic functions.

9. (Previously Presented) A debug client function within an application specific integrated circuit (ASIC), the debug client function being within a field programmable gate array (FPGA), the client debug function comprising:

external communicator logic in communication with a server;

selector logic coupled to a plurality of internal signals that are internal to the application specific integrated circuit (ASIC) and not being exposed via an I/O pin, the selector logic to provide each one of the plurality of internal signals coupled to the field programmable gate array (FPGA) at a particular input point within the debug client function;

comparator logic operable to compare selected ones of the plurality of internal signals at the particular input point with a trigger pattern downloaded from the server through the external communicator logic; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server through the external communicator logic.

10-11. (Cancelled)

12. (Previously Presented) The debug client function of claim 9, wherein the debug client function is programmed by the server.

13. (Cancelled)

14. (Previously Presented) The debug client function of claim 12, wherein the server utilizes the debug client function to debug hardware within at least one of the plurality of logic functions.

15. (Previously Presented) The debug client function of claim 12, wherein the server utilizes the debug client function to debug software within at least one of the plurality of logic functions.

16-22. (Cancelled)

Evidence Appendix

None

Related Proceedings Appendix

None